Atty. Docket No. PIA31071
Serial No: 10/750,489

Amendments to the Claims

Claims 2 and 8 have been previously cancelled. Please cancel Claims 4, 14, and 15, add new Claims 16-24, and amend the remaining claims as follows:

1. (Currently Amended) A method of fabricating an MIM capacitor of high capacitance in a semiconductor device, the method comprising:

depositing an interlayer dielectric film on a metal line;

etching the interlayer dielectric film to form an MIM capacitor forming region;

sequentially depositing a lower electrode layer comprising TiN, an insulator layer and an upper electrode layer on the interlayer dielectric film; and

etching the lower electrode layer, the insulator layer and the upper electrode layer to form an MIM capacitor, wherein a capacitance of the MIM capacitor is determined by ~~controlling~~ a thickness of the interlayer dielectric film.

2. (Canceled)

3. (Currently amended) A method as defined by claim 1, wherein the interlayer dielectric film ~~is made of~~ comprises USG or TEOS.

4. (Cancelled)

5. (Currently amended) A method as defined by claim 1, wherein the insulator layer ~~is made of~~ comprises TaO_2, Al_2O_3, or SiN.

6. (Currently amended) A method as defined by claim 1, wherein the upper electrode layer ~~is made of~~ comprises Ru, Pt, or TiN.

7. (Currently amended) A method of fabricating an MIM capacitor of high capacitance in a semiconductor device, the method comprising:

depositing an interlayer dielectric film on a metal line;

planarizing the interlayer dielectric film;

etching the interlayer dielectric film to form an MIM capacitor forming region;

sequentially depositing a lower electrode layer, an insulator layer and an upper electrode layer on the interlayer dielectric film; and

planarizing the lower electrode layer, the insulator layer and the upper electrode layer by an etch back process to form an MIM capacitor, wherein a capacitance of the MIM capacitor is determined by ~~controlling~~ a thickness of the interlayer dielectric film.

8. (Canceled)

9. (Currently amended) A method as defined by claim 7, ~~wherein~~ further comprising planarizing the interlayer dielectric film ~~is planarized~~ by a chemical mechanical polishing (CMP) process.

10. (Currently amended) A method as defined by claim 7, ~~wherein~~ further comprising planarizing the interlayer dielectric film ~~is planarized~~ by an etch-back process.

11. (Currently amended) A method as defined by claim 7, wherein the lower electrode layer ~~is made of any one of~~ comprises Ti, W, or TiN.

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12. (Currently amended) A method as defined by claim 7, wherein the insulator layer ~~is made of any one of~~ comprises TaO_2, Al_2O_3, or SiN.

13. (Currently amended) A method as defined by claim 7, wherein the upper electrode layer ~~is made of any one of~~ comprises Ru, Pt, or TiN.

14. (Cancelled)

15. (Cancelled)

16. (New) A method as defined by claim 7, further comprising planarizing the interlayer dielectric film by a chemical mechanical polishing (CMP) process.

17. (New) A method as defined by claim 7, further comprising planarizing the interlayer dielectric film by an etch-back process.

18. (New) A method as defined by claim 1, wherein the insulator layer comprises SiN.

19. (New) A method as defined by claim 1, wherein the upper electrode layer comprises Ru.

20. (New) A method as defined by claim 1, wherein the upper electrode layer comprises TiN.

21. (New) A method as defined by claim 7, wherein the lower electrode layer comprises TiN.

22. (New) A method as defined by claim 7, wherein the insulator comprises SiN.

23. (New) A method as defined by claim 7, wherein the upper electrode layer comprises Ru.

24. (New) A method as defined by claim 7, wherein the upper electrode comprises TiN.